AMOLED

Product Specification

Model Name: E544-HC01

Description：5.44” FHD AMOLED

Doc. Version：01

Customer：

□ Approved for Preliminary Specification

□ Approved for Final Specification

■ Approved for Final Specification & Sample

此规格只能符合 AMOLED 单体规格，不含整机规格

Prepared by	Checked by	Approved by

Customer’s Approval

Reversion History			
Reversion. No	Date	Contents	Remark
01	2020-4-15	First version	

Contents

1 Scope

This Specification defines AMOLED manufactured by Voluntary Electron. In the case of any unspecified item, it may require both Voluntary Electron and the party designs this module into its product to work out a solution.

2 Features

2.1 Product Applications

mobile phone, portable GPS, handheld game console…

2.2 Product Features

2.2.1 Display color：16.7M (RGB x 8bits)

2.2.2 Display format：5.44”FHD(1080RGBx1920)

2.2.3 Pixel arrangement：Rendering

2.2.4 Interface：MIPI 4 lanes

2.2.5 Driver IC: RM67199(Raydium)

2.2.6 Touch IC: GT1151

2.2.7 Touch screen：On-Cell

2.2.8 Polarizer: Hard Coating Polarizer

3 Mechanical Specifications

Item	Specification	unit
Dimension outline	69.74*126.60*0.84	mm
Resolution	1080 RGB x 1920 (Rendering)	dots
Active area	67.82 x 120.58	mm
Diagonal size	5.44	inch
Pixel pitch	31.40*62.80	μm
Glass thickness （LTPS/encapsulation glass）	0.20 / 0.30	mm
Weight	(TBD)	g

4 Maximum Rating

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Analog/boost power voltage	VCI	-0.3	-	5.5	V	-
I/O voltage	VDDIO	-0.3	-	5.5	V	-
Power IC Input Voltage	VBAT	-0.3	-	6	V	-
Operating temperature	Top	-20		70	℃	
Storage temperature	Tstg	-30		80	℃	
Power Consumption			2000	2300	mW	

5 Electrical Specifications

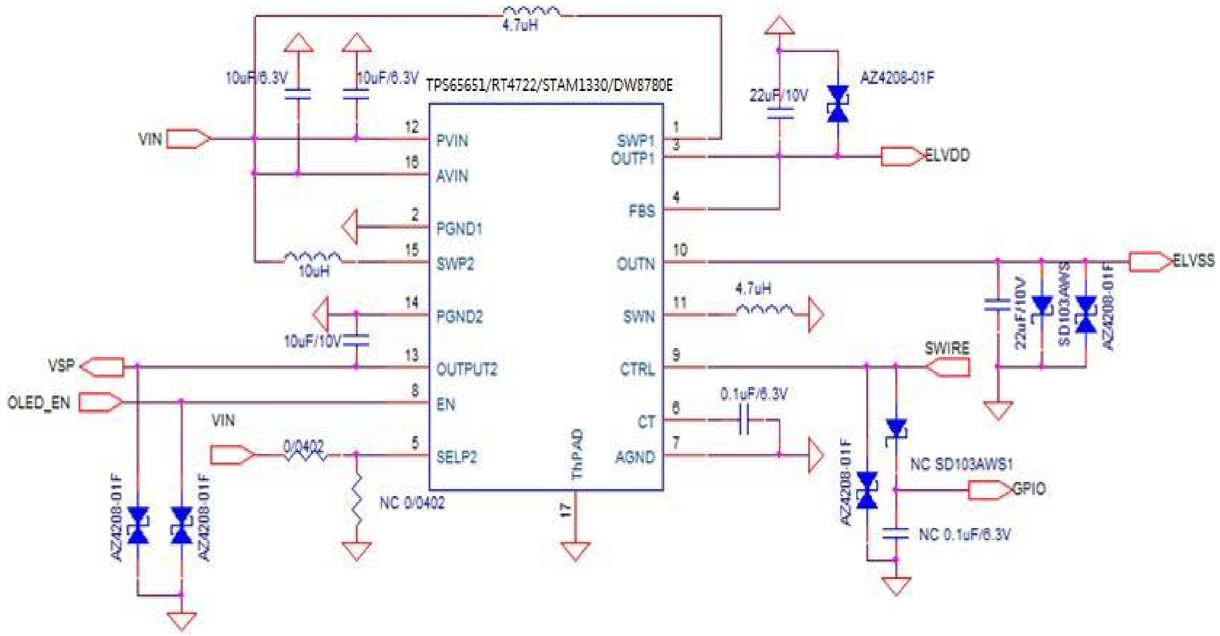
5.1 Electrical Characteristics

5.1.1 Current Characteristic：

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power IC Input Voltage	VBAT	2.9	-	4.5	V	Ref
Digital Power supply	VDDI	1.65	1.8	3.6	V	Ref
Analog Power supply	VCI	2.5	3.3	4.8	V	Ref
TP Power Supply voltage	AVDD	2.7	-	3.6	V	-
TP I/O Digital Voltage	Iovcc	1.65	-	3.6	V	

Mode	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Full White @350 Nits	I_{VBAT}	IVBAT=4V VCI=3.3V VDDIO=1.8V @ Full white 350 nits	-	460	550	mA	-
	I_{VCI}		-	2	3	mA	-
	I_{VDDIO}		-	50	65	mA	-
TP Normal Operation	Iopr	AVDD=3.3V Iovcc =1.8V		16		mA	-
TP Monitor	Imon			0.6		mA	-
TP Sleep	Islp			40		uA	-

5.1.2 Application circuit：



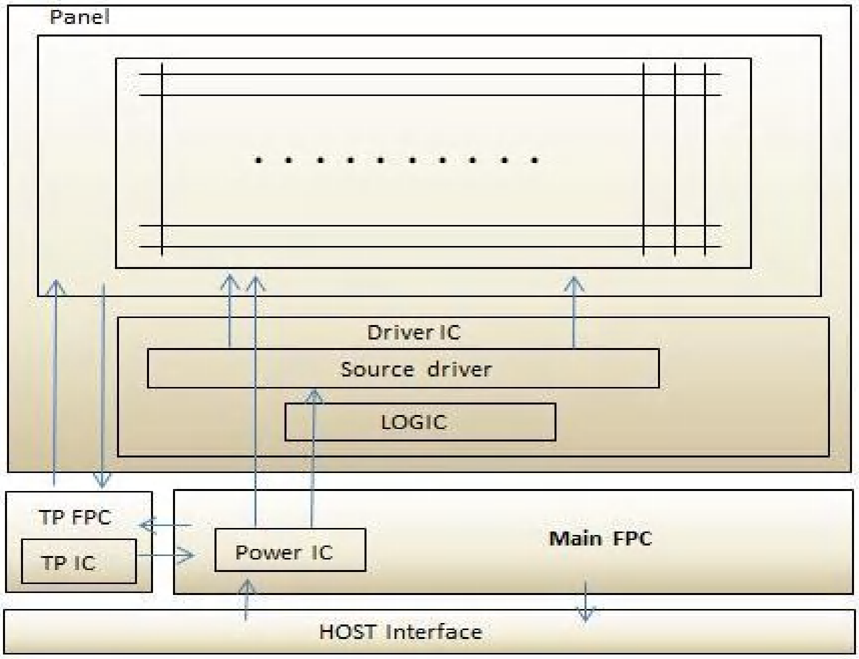
5.2 I/O Connection and Block Diagrams

5.2.1 I/O Connection

#	Pin_name	I/O	Description
1	GND	Power	The power ground
2	GND	Power	The power ground
3	GND	Power	The power ground
4	VBAT	Power	Power IC Input Voltage
5	VBAT	Power	Power IC Input Voltage
6	VBAT	Power	Power IC Input Voltage
7	VBAT	Power	Power IC Input Voltage
8	VBAT	Power	Power IC Input Voltage
9	GND	Power	The power ground
10	VPP	Power	Power supply for OTP. Leave the pin to open when not in use.
11	NC	-	No connection
12	GND	Power	The power ground
13	D3P	I	MIPI DSI data3+

14	D3N	I/O	MIPI DSI data3-
15	GND	Power	The power ground
16	D0P	I/O	MIPI DSI data0+
17	D0N	I/O	MIPI DSI data0-
18	GND	Power	The power ground
19	CLKP	I	MIPI DSI clock+
20	CLKN	I	MIPI DSI clock-
21	GND	Power	The power ground
22	D1P	I/O	MIPI DSI data1+
23	D1N	I/O	MIPI DSI data1-
24	GND	Power	The power ground
25	D2P	I/O	MIPI DSI data2+
26	D2N	I/O	MIPI DSI data2-
27	GND	Power	The power ground
28	RESX	I	This signal will reset the device and must be applied to properly initialize the chip. Active low.
29	VDDIO	Power	Driver IC digital I/O supply
30	VCI	Power	Driver IC analog supply
31	TE	O	Tear effect output
32	GND	Power	The power ground
33	TSP_AVDD	Power	TP IC digital power supply
34	TSP_DVDD	Power	TP IC digital I/O supply
35	TSP_SDA	I/O	I2C Data Input & Output
36	TSP_SCL	I/O	I2C Clock Input
37	TSP_RESET	I	External Reset,Low is Active
38	TSP_ATTN	I	Interrupt request to the host, or Wakeup request from the host.
39	ID	O	Panel ID

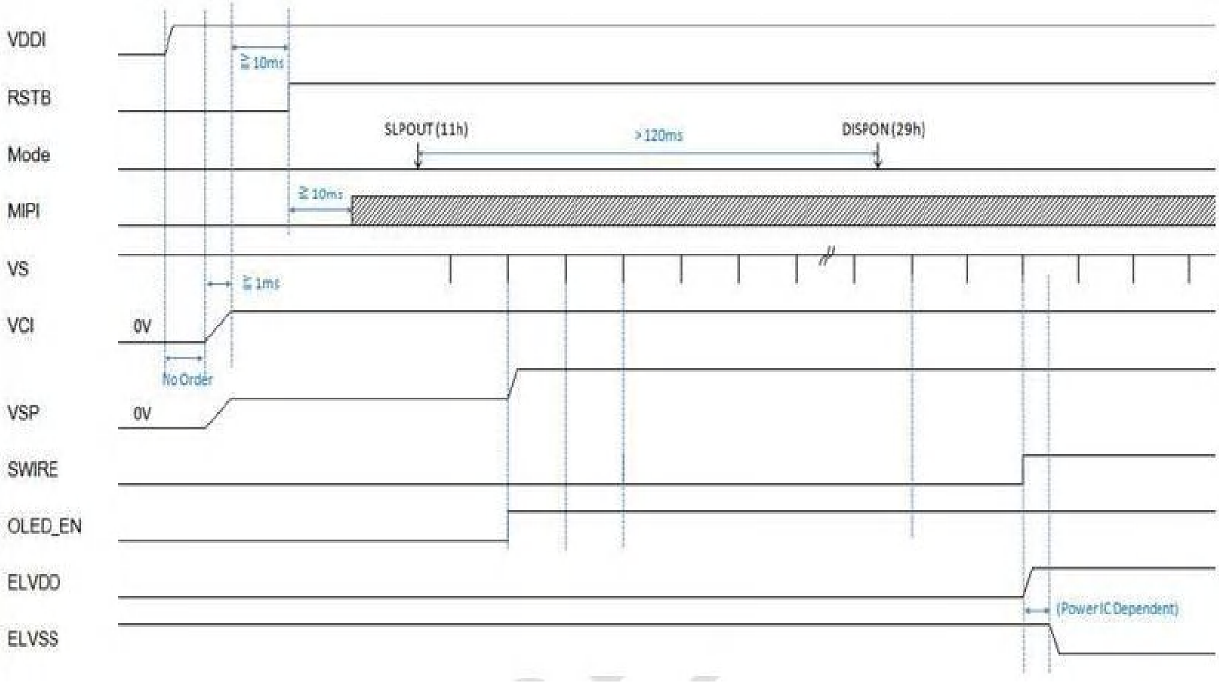
5.2.2 Display Module Block Diagram



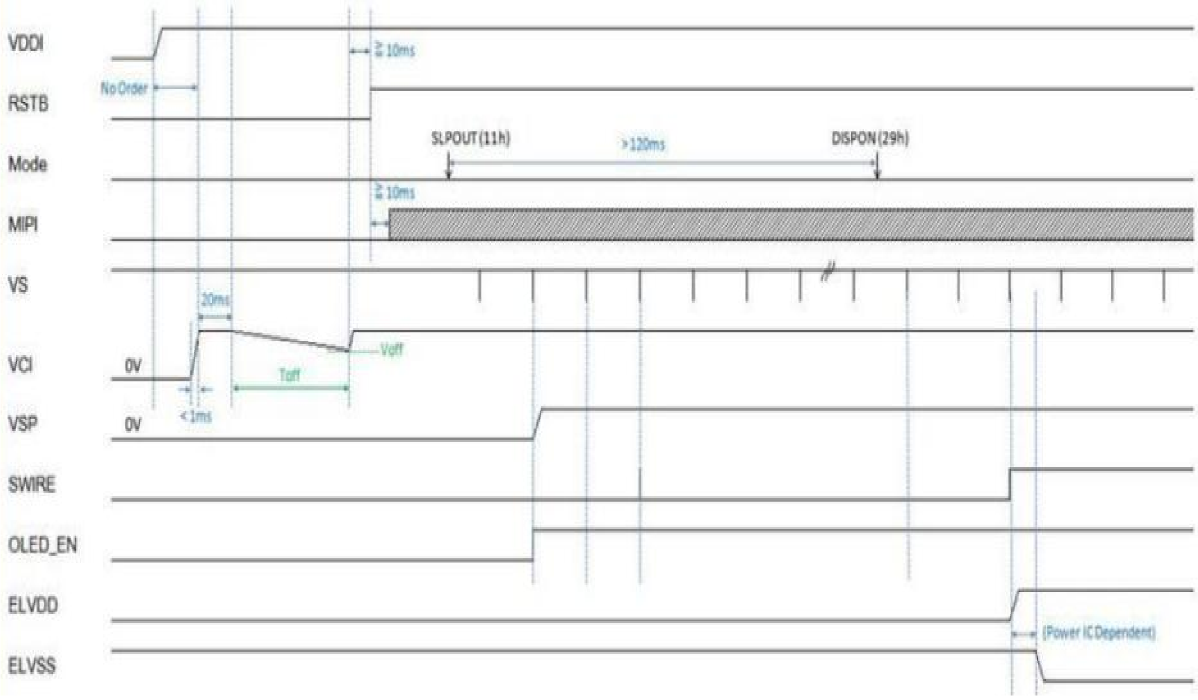
5.3 Recommended Operating Sequence

5.3.1 Power on sequence

1. Power ON for Normal VCI Case: Tr>1ms



2. Power ON for fast VCI Case: Tr<1ms



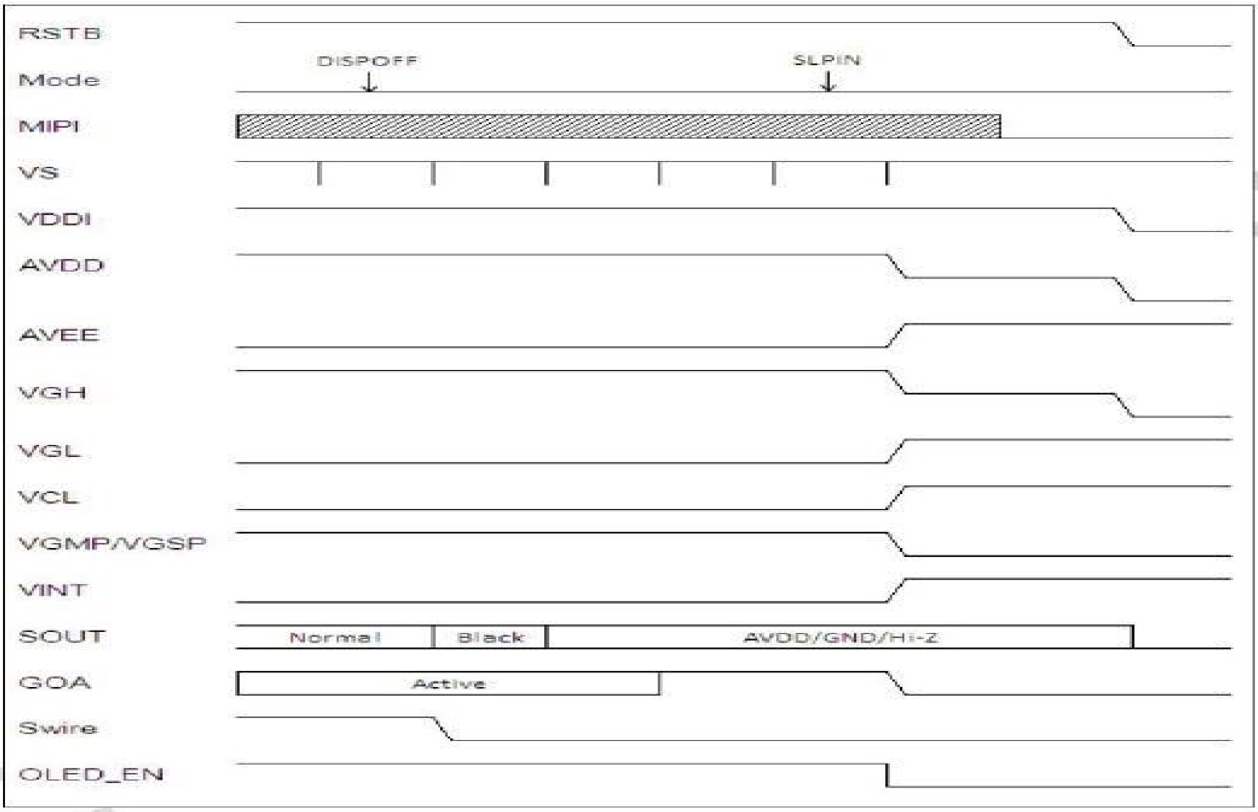
Note: If VCI's rising time is smaller than 1ms,it is suggested to use VCI H-L-H sequence to avoid the start-up issue due to fast VCI ramp up.

--the 1st H is suggested to be 20ms

--the L period is the time that can make Voff in between 2.6V and 1.5V.

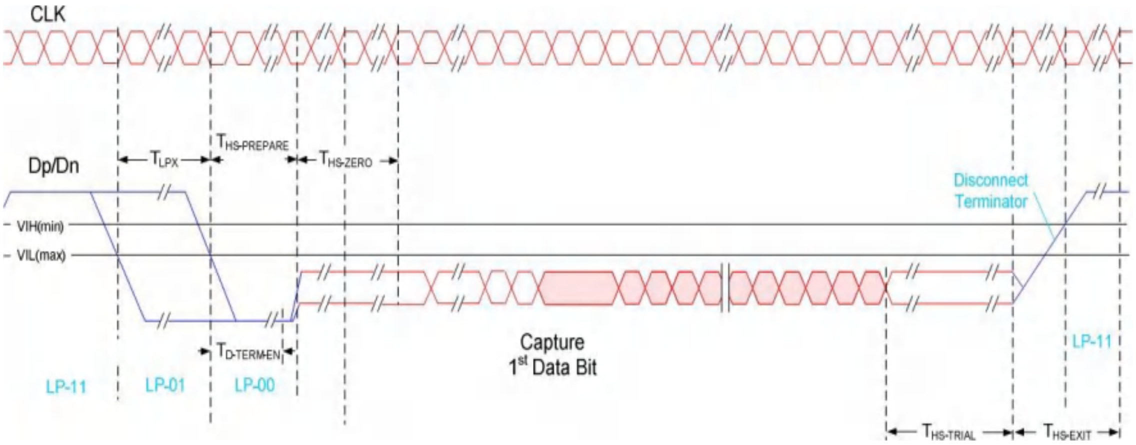
(for example ,when the discharge time is 20ms and 200ms for VCI to drop below 2.6V and 1.5V, respectively. Then the Toff is suggested to be>20ms and <200ms.)

5.3.2 Power off sequence

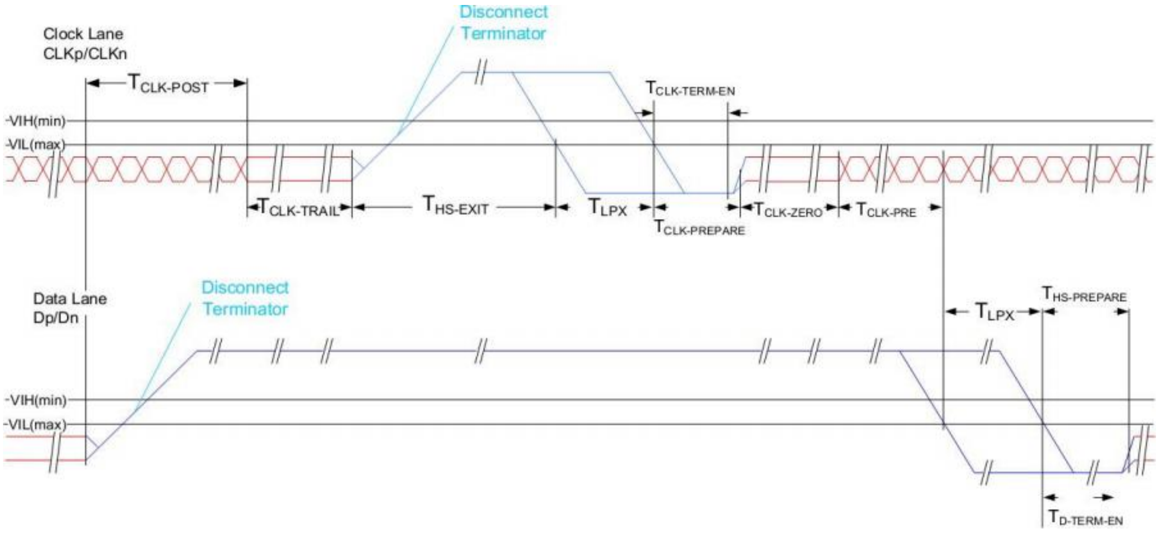


5.4 AC Characteristics (MIPI)

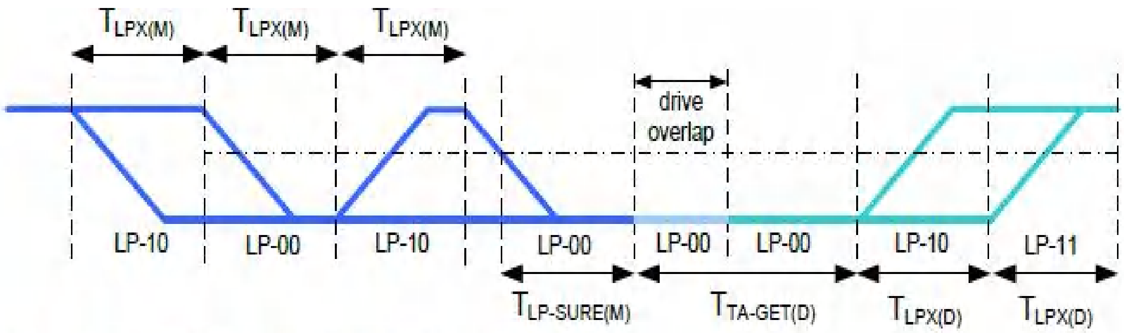
5.4.1 HS Data Transmission Burst



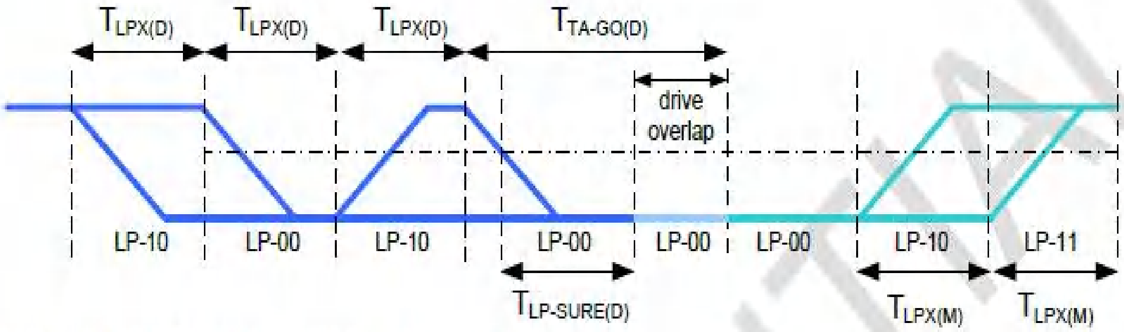
5.4.2 HS Clock Transmission



5.4.3 Turnaround Procedure

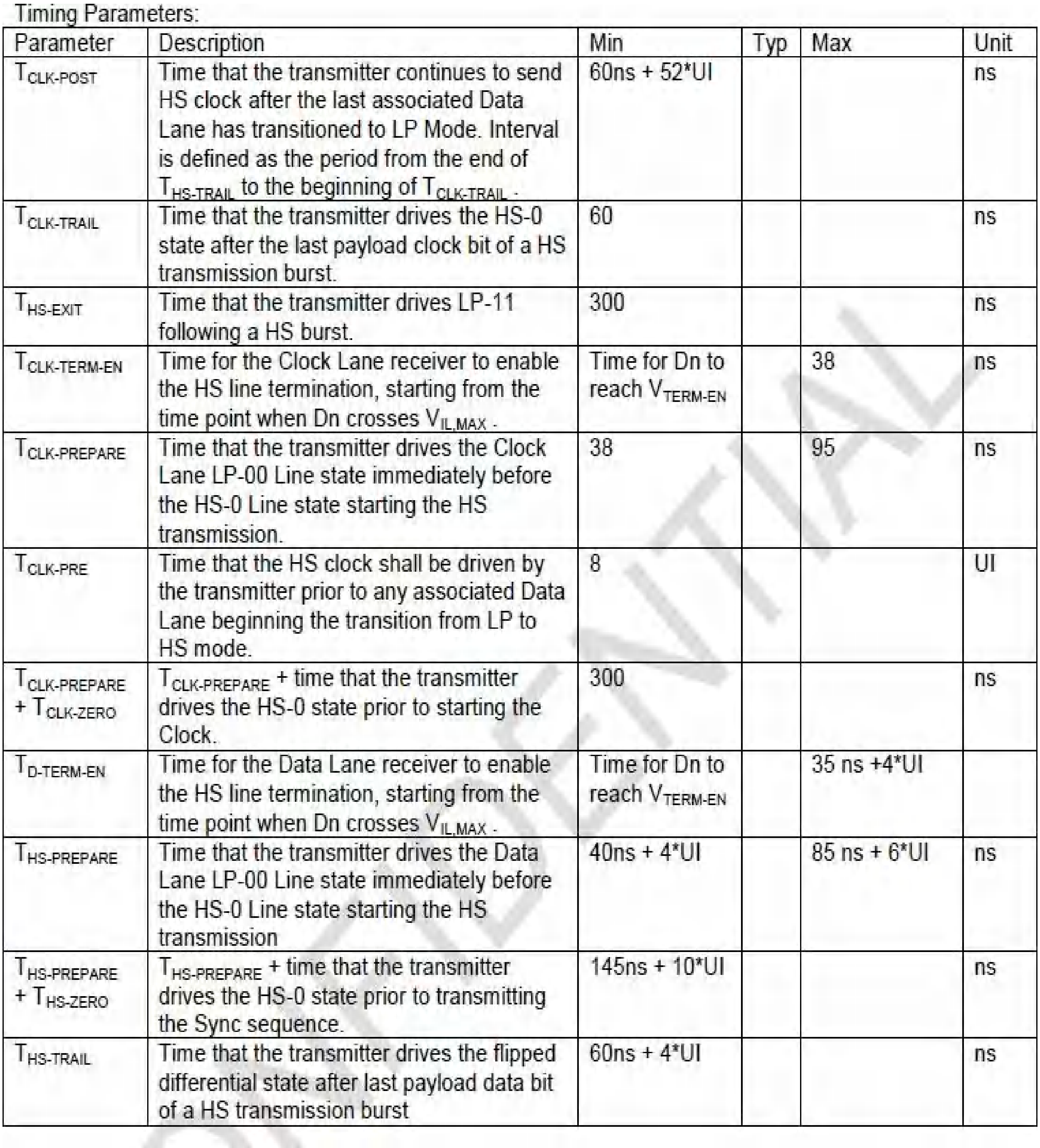


Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

5.4.4 Timing Parameters



Timing Parameters:

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	300			ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns +4*UI	
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85 ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4*UI			ns

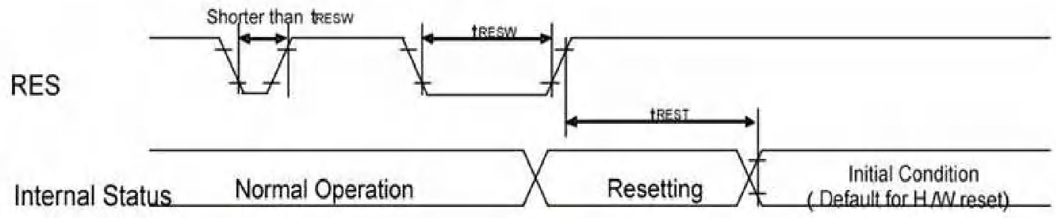
Low Power Mode :

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{LPX(M)}$	Transmitted length of any Low-Power state period of MCU to display module	50		**150**	ns	1,2
$T_{TA\text{-}SURE(M)}$	Time that the display module waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(M)}$		$2^*T_{LPX(M)}$	ns	2
$T_{LPX(D)}$	Transmitted length of any Low-Power state period of display module to MCU	50		**150**	ns	1,2
$T_{TA\text{-}GET(D)}$	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		$5^*T_{LPX(D)}$		ns	2
$T_{TA\text{-}GO(D)}$	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		$4^*T_{LPX(D)}$		ns	2
$T_{TA\text{-}SURE(D)}$	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	$T_{LPX(D)}$		$2^*T_{LPX(D)}$	ns	2

NOTE:

1. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
2. Transmitter-specific parameter

5.4.5 Timing requirements for RESETB



Reset input timing:

IOVCC=1.65 to 3.6V, VDD=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85℃

Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse width	RESX	10	-	-	-	µs
t_{REST}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-		-	120	When reset applied during Sleep out mode	ms

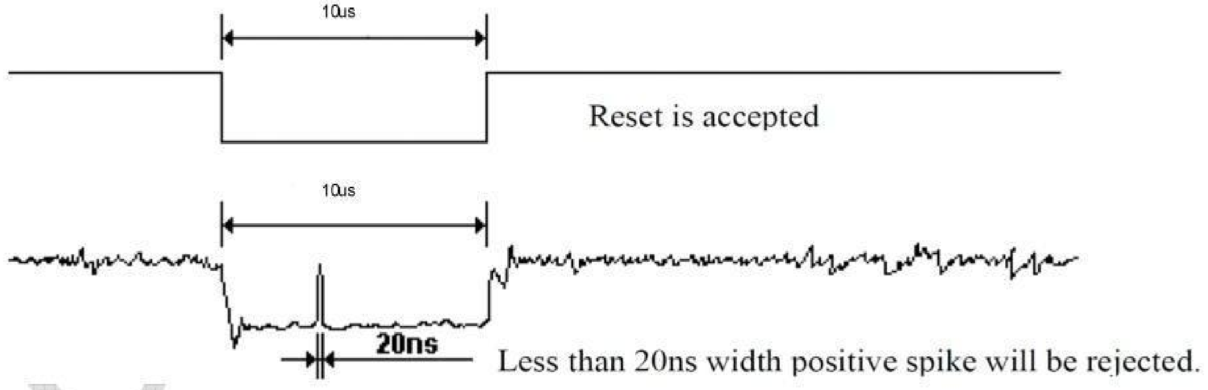
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 10µs	Reset
Between 5µs and 10µs	Reset starts (It depends on voltage and temperature condition.)

Note 2. During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

Note 3. During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4. Spike Rejection also applies during a valid reset pulse as shown below:



Note 5. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6 Electro-Optical Specification

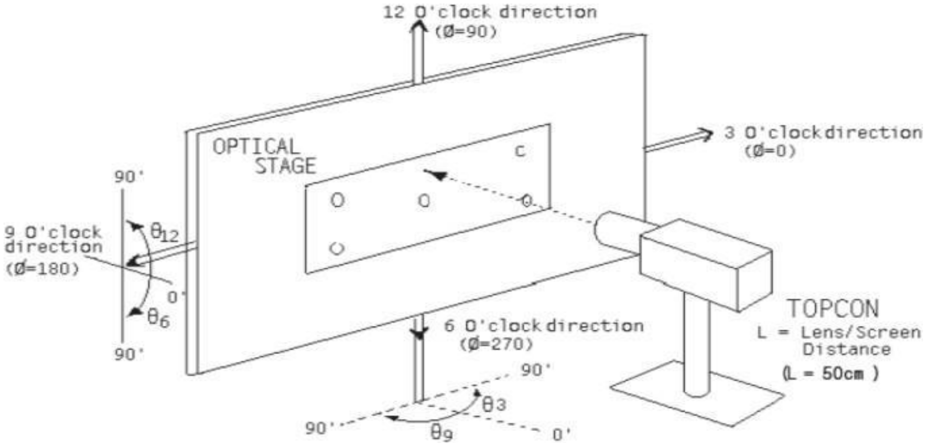
Item		Symbol	Conditions	Min.	Typ.	Max.	Unit	Remark
Brightness			L255	315	350	385	cd/m^2	Note1
Brightness Uniformity			L255	75		-	%	Note2
Contrast Ratio		CR	Normal to surface	60,000		-	-	Note3
CIE Chromaticity	White	x	Normal to surface	0.275	0.295	0.315	-	
		y		0.285	0.305	0.325	-	
	Red	x		0.66	0.69	0.72	-	
		y		0.28	0.31	0.34	-	
	Green	x		0.195	0.235	0.275	-	
		y		0.68	0.72	0.76	-	
	Blue	x		0.113	0.143	0.173	-	
		y		0.014	0.044	0.074	-	
Color Gamut			vs. NTSC	90	105		%	
Viewing angle			U/D/L/R CR≥1000	80		-	°	
Color shift (JNCD)			@ 45 degree			6		Note4
Cross-talk				-	-	2	%	Note5
Gamma			V(Gray)= 48,72,104,132,164, 192,224,255	2.0	2.2	2.4	-	
Response time				-	-	2	ms	Note6
Flicker			Normal Θ=Φ=0°			-40	dB	Note 7
Image Retention						3	min	Note 8
Image Sticking						3	hrs	Note 9
Color Uniformity			Full White Δu'v'			0.012		Note 10

※亮度均匀度以 L255进行测量。

※Mura 检测在 L128 状态进行判别

Note1: Temp.25℃, （Angle、distance）

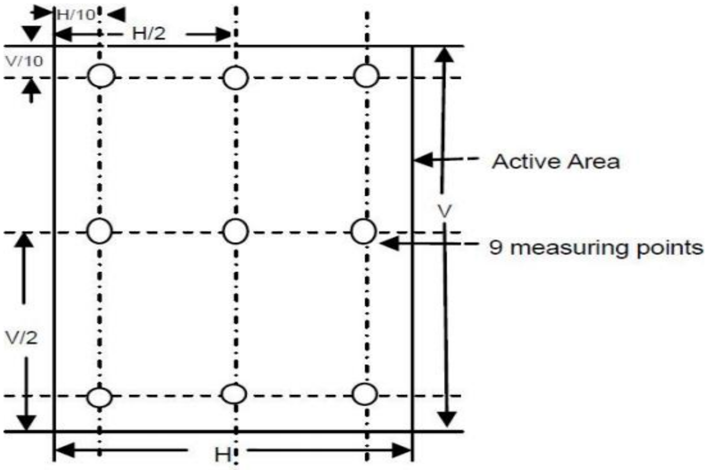
Environmental conditions：Temp.25℃±3℃，65±20%RH，Dark Room 。
Distance of OLED display center to measuring machine is 50cm。



Note2: Brightness Uniformity definition

Measure 9 points of Display Brightness,

$$\text{Luminance uniformity} = \frac{(\text{Min Luminance of 9 points})}{(\text{Max Luminance of 9 points})} \times 100\%$$



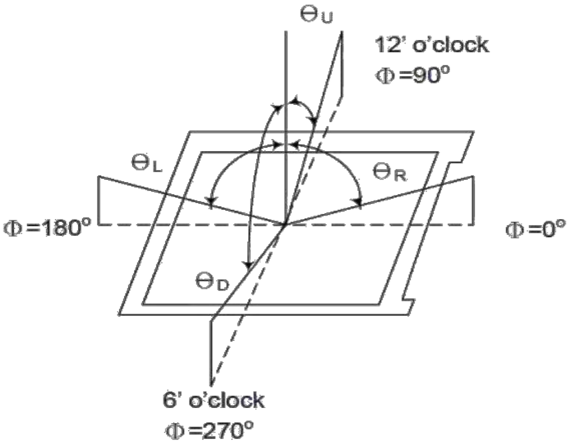
Note3: Contrast Ratio

Dark Room C.R=LW/LB

LW: full white brightness of display center P0;

LB : full black brightness of display center P0.

Contrast Ratio Uniformity = CRmin / CRmax



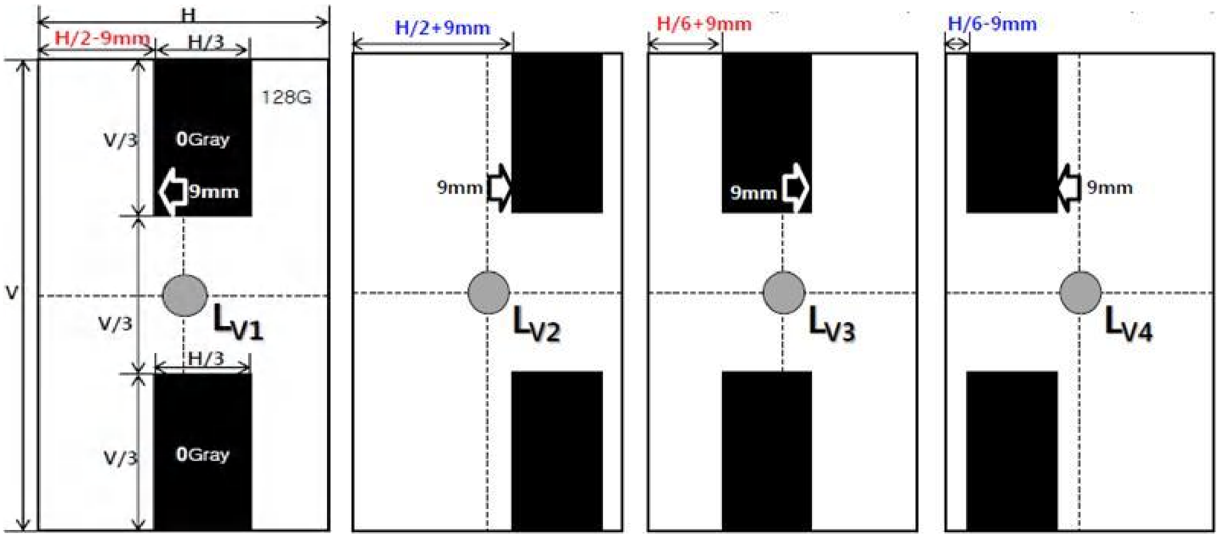
Note4: Color Shift JNCD

- For JNCD measure:
- Fix on the white pattern,
- On the condition θ=0 F=0°, we can get the color coordinate (u1', v1') and on θ F=45° we can get another color coordinate (u2', v2')
- Delta = Square Root((u2'-u1')^2 + (v2'-v1')^2)
- JNCD stands for "Just Noticeable Color Difference"
- For the (u', v') color space JNCD=0.0040.
- 4 JNCD means Delta u'v'<0.016

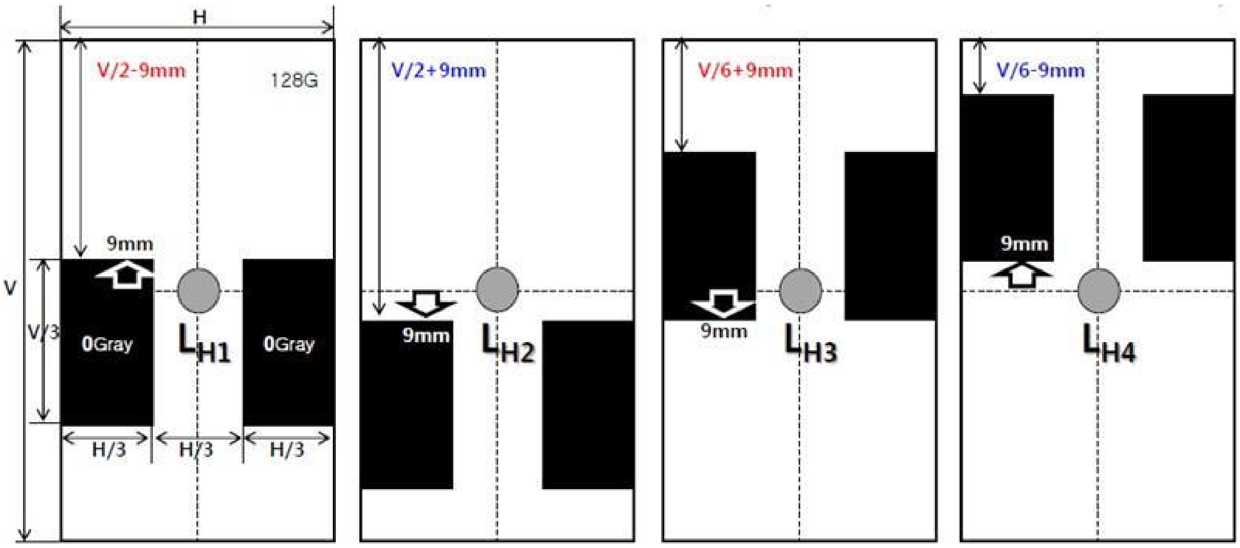
Note5: Cross-talk

22% black window， 128 gray background. Pattern Left/Right 9mm shift

$$Crosstalk(V) = \max\left(\left| \frac{L_{V1} - L_{V2}}{L_{V2}} \right| \times 100, \left| \frac{L_{V3} - L_{V4}}{L_{V4}} \right| \times 100 \right)$$



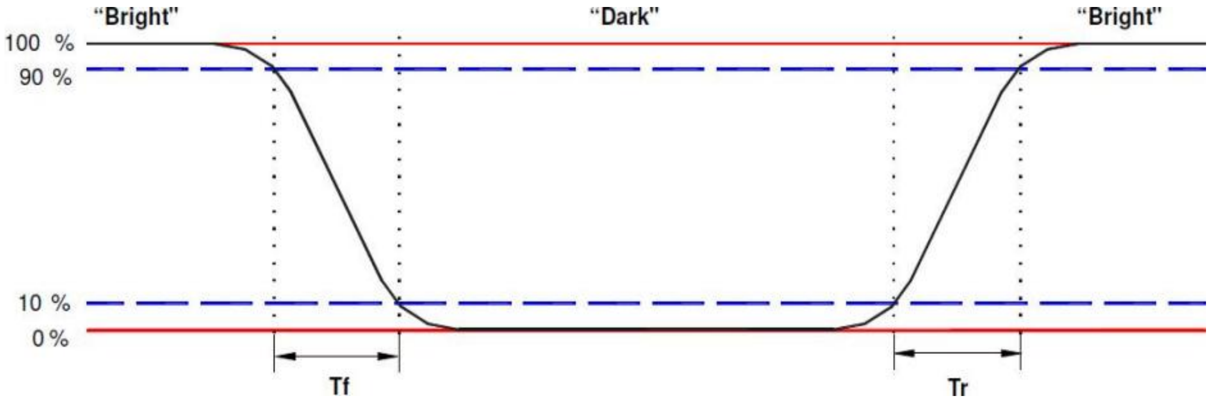
$$Crosstalk(H) = \max\left(\left|\frac{L_{H1}-L_{H2}}{L_{H2}}\right|\times 100, \left|\frac{L_{H3}-L_{H4}}{L_{H4}}\right|\times 100\right)$$



Note6: Response Time

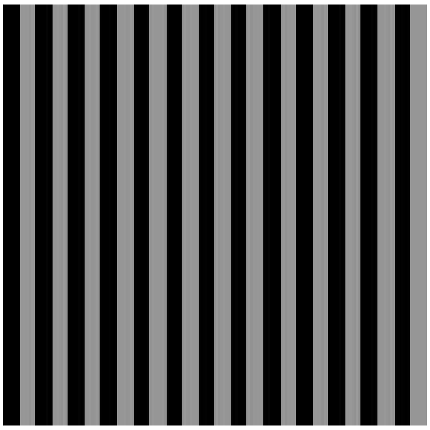
Response time=Pixel turn on and turn off time (White<=>Black).

It is measuring transition time from 10% to 90% of luminance.



Note 7: Flicker

Suggested Instruments: **Konica Minolta CA-310** or **Klein Instruments K-8**



Odd row : **L0** Black
Even row : **L186** gray level

Flicker Test Pattern

The flicker level is defined by **Fast Fourier Transformation (FTT)** as follows:

$$Flicker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad \text{(dB)}$$

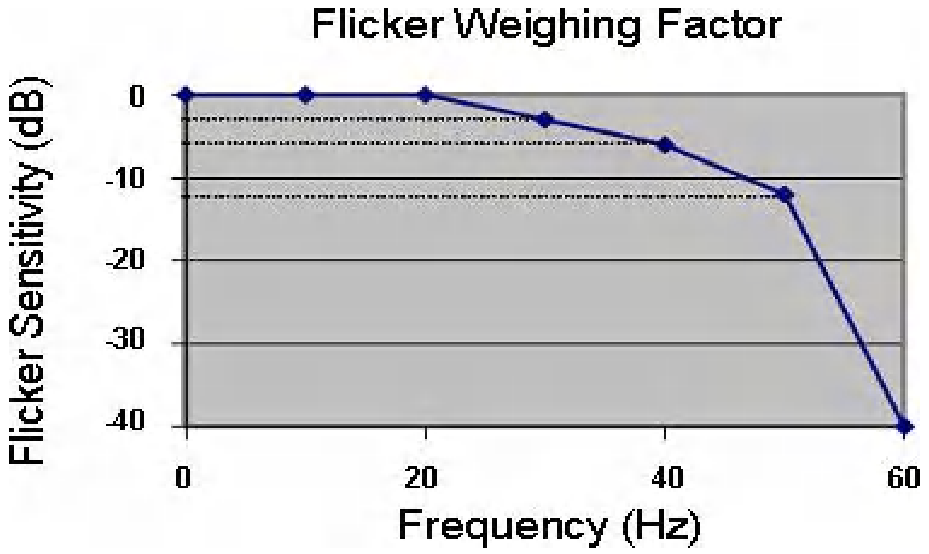
Where

f_{FFTC}(n) is the n-th FFT coefficient.

f_{FFTC}(0) is the 0-th FFT coefficient which is DC component.

FS(Hz) is the flicker sensitivity as a function of frequency.

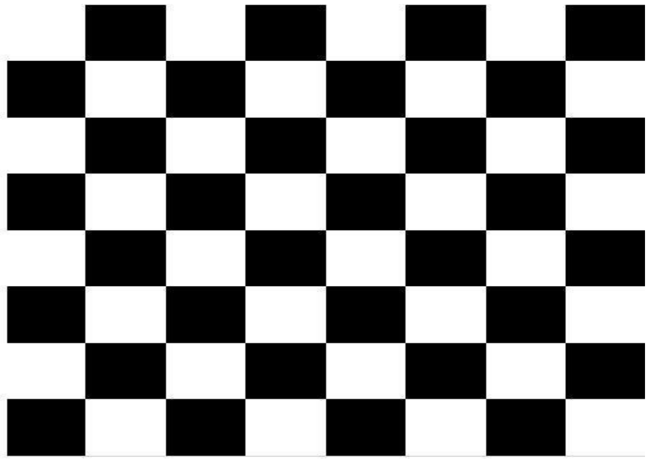
The peak flicker level shall be reported based on the calculation using above formula in which FS(Hz) is determined by the flicker weighing factor shown below.



Flicker Weighing Factor

Note8: Image Retention

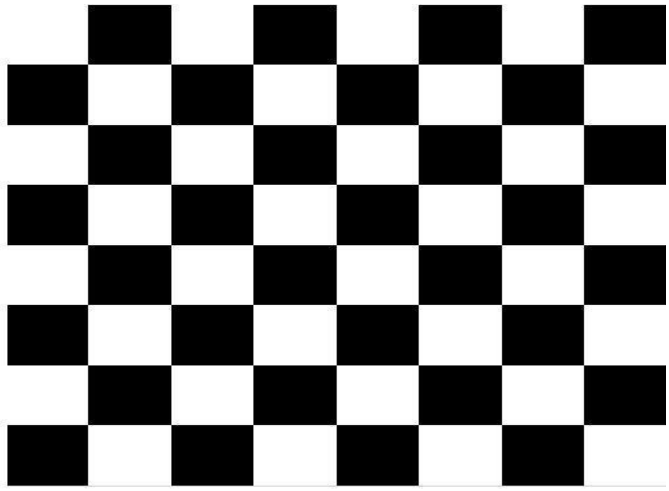
Using chessboard pattern (8 * 8) light on 1hr, and switch to 127 gray. The Image retention should not be seen after 3 mins.



Note9: Image Sticking

Using chessboard pattern (8 * 8) light on 3 hrs, and switch to 127 gray.

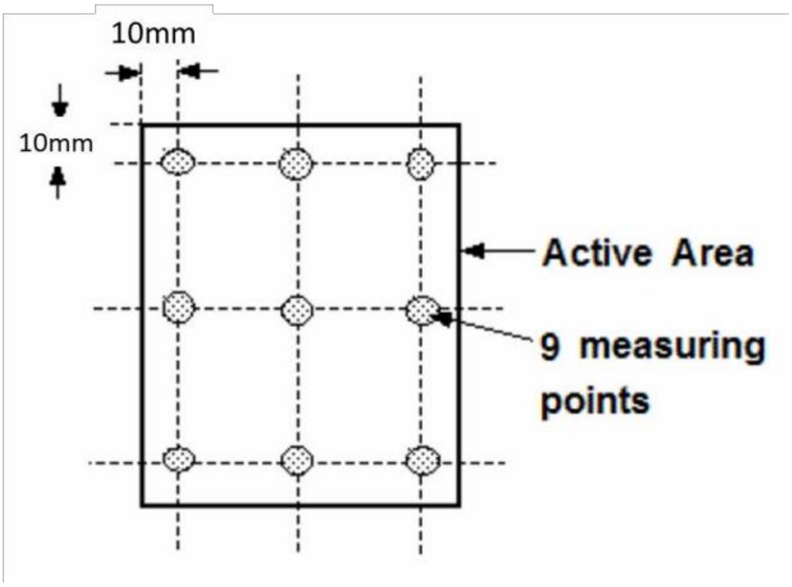
The Image Sticking should not be seen after 60 min with ND02 filter (image sticking disappear after stewing).



Note10: Color Uniformity

Total 9 measure points should set as shown in the following figures. The CIE 1967 Standards shall be used.The color difference is calculated by using following formula:

Max（△u'v'）（the max △u'v' value between two random point of 9 point）



7 Reliability

7.1 Environmental Test

No	Item	Conditions	Quantity	Note
1	High Temperature Operating (HTO)	70℃/48hrs	5pcs	After testing - No clearly visible defects or remarkable deterioration of display quality. However, any polarizer's deteriorations by the high temperature/ High humidity test are permitted. - No function-related abnormalities.
2	Low Temperature Operating (LTO)	-20℃/48hrs	5pcs	
3	High Temperature Storage (HTS)	80℃/48hrs	5pcs	
4	Low Temperature Storage (LTS)	-40℃/48hrs	5pcs	
5	High Temperature / High Humidity Operating (HTHHO)	60℃ /93%R.H./96hrs	5pcs	
6	High Temperature/High Humidity Storage (HTHHS)	60℃ /93%R.H./96hrs	5pcs	

7.2 Electrical Test

No	**Item**	**Conditions**	**Note**
1	Air discharged Criteria C	±8kV	After testing - Hard defect should not happen. - If it would be recovered to normal state after resetting, it would be judged as a good state. (Class C)
2	Contact discharged Criteria C	±4kV	

7.3 Mechanical Test

No	**Item**	Conditions	**Note**
1	Glass Strength Test	4PB，B10 >100MPa （stress）	
2	Ball Drop Test	0.2J @ center 32g, 45cm 屏幕中心 3 次,四个角各 1 次	Module with CG
3	Drop Test	10 Drops: 6 surfaces / 3edges / 1corner/ for Carton test & Gift Box Test 0~9kg /92cm 9.2kg~18.2kg /76cm 18.3kg~27.2kg /61cm 27.3kg~45.4kg /46cm	Package
4	Vibration Test	Accleration:1.48Grms 5~100Hz 0.015G*2/Hz / 100~200Hz -6dB/Oct / 200Hz 0.0038G*2/Hz / Test Time : 30 min	Package

8 Handling Precautions

8.1 When cleaning ITO pad, avoid using hard and abrasive material or corrosive solution

8.2 Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity

8.3 Strong impact & pressure on module and packing is prohibited

8.4 Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display

8.5 Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available

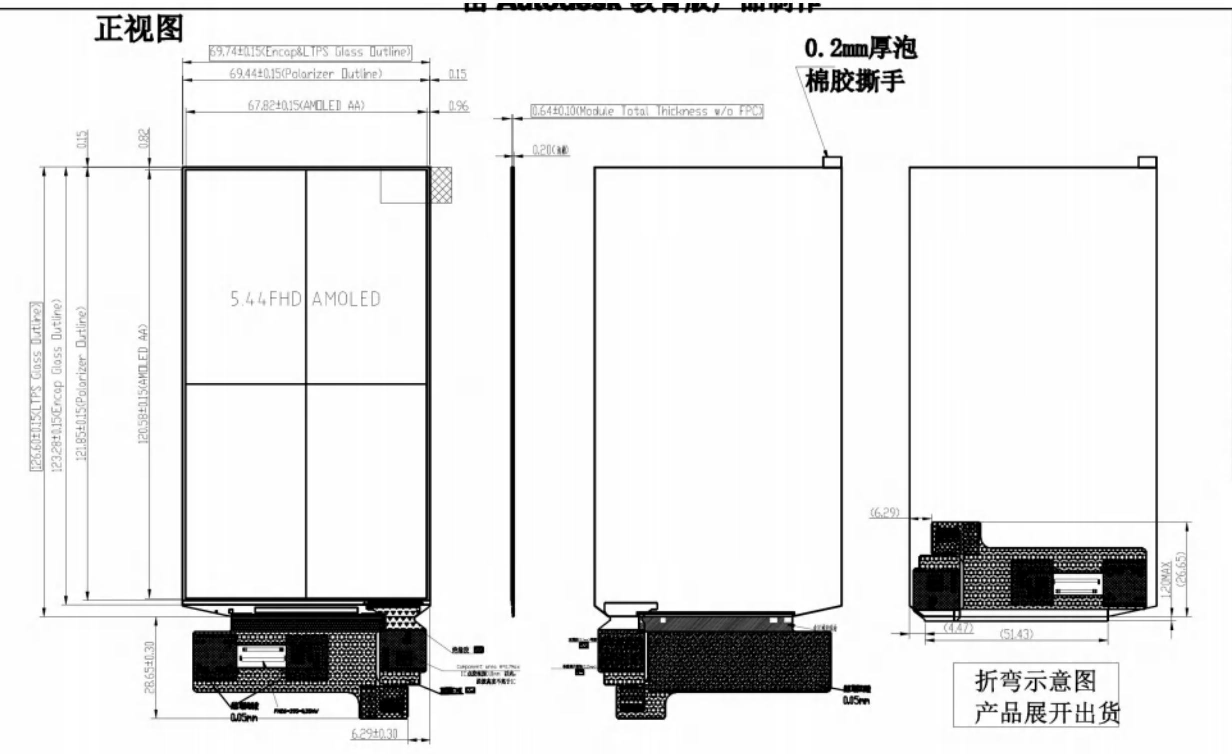
8.6 Image sticking may occur if an image displays for an extended period of time

8.7 When interfered by system's overall mechanical design, an abnormal display may occur

8.8 After considering emitting energy, you should plan your design to satisfy EMI standards.

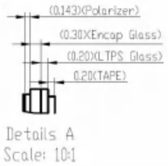
8.9 Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.

9 Outline Dimension Drawing



CN1			
No.	Pin Define	No.	Pin Define
1	GND1	21	GND8
2	GND2	22	D1P
3	GND3	23	D1N
4	VBAT1	24	GND9
5	VBAT2	25	D2P
6	VBAT3	26	D2N
7	VBAT4	27	GND10
8	VBAT5	28	RESX
9	GND4	29	VDDIO
10	VPP	30	VCI
11	NC1	31	TE
12	GND5	32	GND11
13	D3P	33	TSP_AVDD_3.3V
14	D3N	34	TSP_DVDD_18V
15	GND6	35	TSP_SDA
16	D0P	36	TSP_SCL
17	D0N	37	TSP_RESET
18	GND7	38	TSP_ATTN
19	CLKP	39	ID
20	CLKN		

技术要求:
1) 玻璃显示模式:AMOLED 5.44″ FHD
   视角: All
   分辨率: 1080 (RGB) X1920 DOTS
   驱动芯片型号: RM67199
   TP驱动芯片: GT1151
   玻璃型号: 和辉光电
2) **未注尺寸公差及装配公差:±0.2mm**
3) **带*为重点尺寸**
4) **材料及工艺要求符合RoHS** ROHS
5) **建议模组背面跟机壳在厚度方向预留0.3mm间隙**
6) **建议VA视窗比模组AA单边大0.3mm**



Details A
Scale: 10:1

▨ **黄胶纸**
■ **双面胶**
■ **导电胶**
▨ **单层区**
▨ **屏蔽膜**

显示模组单体		
	接口模式	MIPI VIDEO 模式
	工作电压	VCC:2.8V, IOVCC:1.8V
	平均亮度规格	350cd/m2(typ),315/m2(min)
	中心点色度	色度XY以签样为中心值±0.03;
	背光电路参数	
	连接器	WP7B-S040VA1
	工作温度	-20° C TO 60° C
	储存温度	-30° C TO 70° C

V1.2				设计	
V1.1				检查	
V1.0	初始图纸	ZY	2020.08.25	批准	
版本	变更履历	签名	日期	其他	

图纸名称

模组图纸

项目型号

5.5_FHD_AMOLED显示屏

单位	mm	比例	1:1
第三视角		表	1/1

10 Packing Specification